CLAIM AMENDMENTS

1. (previously presented) A spread spectrum digital communication receiver, the receiver comprising:

an input memory buffer for storing samples of an input signal;

a code generator circuit for generating a regenerated user code;

a device for the estimation of a channel delay profile energy, for computing the time delays and amplitudes of each received multi-path component of said input signal;

a plurality of fingers; and

a finger allocation unit for processing said channel delay profile energy in order to select the strongest multi-path components of said input signal and allocate them to said fingers;

wherein the device for the estimation of a channel delay profile energy comprises:

a basic correlator having a first input for sequentially reading from a memory location of said input memory buffer a plurality of samples of said input signal, a second input for receiving from said code generator circuit a regenerated user code, and an output terminal for generating, by means of a correlation operation between said plurality of samples of said input signal and said regenerated user code, a value of said channel delay profile energy; and

a memory controller circuit for addressing said input memory buffer so that said first input of said basic correlator is successively fed with the content of the memory locations of said memory buffer, each addressing operation corresponding to a new correlation operation of said basic correlator for the computation of a new value of said channel delay profile energy.

2. (previously presented) The receiver according to claim 1, wherein the values of said channel delay profile energy are progressively stored in a profile accumulation memory.

3. (previously presented) The receiver according to claim 2, wherein said memory controller circuit addresses said profile accumulation memory so that the reading operations of said basic correlator from said input memory buffer and the writing operations into said profile accumulation memory are handled by the memory controller circuit.

4. (previously presented) The receiver according to claim 3, wherein said memory controller circuit updates the addressing of said input memory buffer and said profile accumulation memory every NC chips, where NC is equal to the integration window size, changing the reading and writing positions of said basic correlator.

5. (previously presented) The receiver according to claim 3, wherein, when the last memory location of both said input memory buffer and said profile accumulation memory is reached, the addressing restarts circularly on a first location of both memories.

6. (previously presented) The receiver according to claim 3, wherein said basic correlator is time multiplexed, at a multiple of the chip frequency, between a plurality of memory locations of said input memory buffer and of said profile accumulation memory.

7. (previously presented) The receiver according to claim 2, wherein said delay profile energy is obtained by accumulating the energies of several delay profiles.

8 - 9. (canceled)

10. (previously presented) A spread spectrum digital communication receiver, the receiver comprising:

a code generator circuit for generating a regenerated user code;

a memory buffer for storing samples of said regenerated user code;

a device for the estimation of a channel delay profile energy, for computing the time delays and amplitudes of each received multi-path component of an input signal received by said receiver;

a plurality of fingers; and

a finger allocation unit for processing said channel delay profile energy in order to select the strongest multi-path components of said input signal and allocate them to said fingers; wherein the device for the estimation of a channel delay profile energy comprises:

a basic correlator having a first input for receiving said input signal and a second input for sequentially reading from a memory location of said memory buffer a plurality of samples of said regenerated user code, and an output terminal for generating, by means of a correlation operation between said input signal and said plurality of samples of said regenerated user code, a value of said channel delay profile energy; and

a memory controller circuit for addressing said memory buffer so that said second input of said basic correlator is successively fed with the content of the memory locations of said memory buffer, each addressing operation corresponding to a new correlation operation of said basic correlator for the computation of a new value of said channel delay profile energy.

11. (previously presented) The receiver according to claim 10, wherein the values of said channel delay profile energy are progressively stored in a profile accumulation memory.

12. (previously presented) The receiver according to claim 11, wherein said memory controller circuit addresses said profile accumulation memory so that the reading operations of said basic correlator from said memory buffer and the writing operations into said profile accumulation memory are handled by the memory controller circuit.

13. (previously presented) The receiver according to claim 12, wherein said memory controller circuit updates the addressing of said memory buffer and said profile accumulation memory every NC chips, where NC is the integration window size, changing the reading and writing positions of said basic correlator.

14. (previously presented) The receiver according to claim 12, wherein, when the last memory location of both said memory buffer and said profile accumulation memory is reached, the addressing restarts circularly on a first location of both memories.

15. (previously presented) The receiver according to claim 12, wherein said basic correlator is time multiplexed, at a multiple of the chip frequency, between a plurality of memory locations of said memory buffer and of said profile accumulation memory.

16. (previously presented) The receiver according to claim 12, wherein said delay profile energy is obtained by accumulating the energies of several delay profiles.

17. (currently amended) A method for the estimation of the channel delay profile energy in a spread spectrum digital communication receiver of the type comprising a code generator circuit for generating a regenerated user code and a memory buffer for storing samples of said regenerated user code and having a first output port for feeding a plurality of fingers with a corresponding plurality of samples of the regenerated user code and a second output port, comprising the steps of:

a) sequentially reading a first plurality of samples of the regenerated user code from the second output of said memory buffer;

b) correlating said plurality of samples of said regenerated user code with an input signal y(k) for generating a first value of the channel delay profile energy;

c) updating the reading position on said input memory buffer every_NC_chips_where_NC_is_the_integration_window_size for reading a further plurality of samples of the regenerated user code;

d) correlating said further plurality of samples of said regenerated user code with said input signal for generating a further value of the channel delay profile energy, said generated value of the channel delay profile energy being stored in a profile accumulation memory; and

e) repeating the steps c) to d) in order to compute all the values of the channel delay profile.

18. (previously presented) The method according to claim 17, further comprising the step of storing each generated value of said channel delay profile energy in a profile accumulation memory.